WHAT IS CLAIMED IS:

1. A semiconductor device having a capacitor that includes a first electrode layer, a dielectric layer, and a second electrode layer is formed on a semiconductor substrate that exposes lower wiring and a lower insulating film, comprising:

an interlayer insulating film including a first electrode opening that exposes the lower wiring, and a second electrode opening adjacent to the first electrode opening that exposes a predetermined region of the lower wiring;

a first electrode formed in the first electrode opening so that the first electrode fills the first electrode opening;

a dielectric layer formed along inner walls and defining the second electrode opening;

a second electrode formed on the dielectric layer so that the second electrode fills the second electrode opening;

upper wiring formed over at least a portion of the second electrode; and

an upper insulating film formed on the interlayer insulating film surrounding the upper wiring.

2. The semiconductor device of claim 1, wherein the first electrode and the second electrode are made of copper.

3. The semiconductor device of claim 1, wherein the upper wiring and the lower wiring are made of copper.

4. The semiconductor device of claim 1, wherein the dielectric layer is formed by layering silicone oxide and silicon nitride.

5. The semiconductor substrate of claim 1, wherein the first electrode and the second electrode are each formed to have a plurality of branches that extend from a base portion.

6. A method for fabricating a semiconductor device, comprising:

forming an interlayer insulating film on a semiconductor substrate that exposes lower wiring and a lower insulating film;

selectively etching the interlayer insulating film to form a first electrode opening that exposes the lower wiring;

forming a first electrode in the first electrode opening so that the first electrode opening is filled;

selectively etching the interlayer insulating film at a region adjacent to the first electrode to form a second electrode opening;

forming a dielectric layer along inner walls that define the second electrode opening;

forming a second electrode on the dielectric layer to fill the second electrode opening; and

forming upper wiring on at least a portion of the second electrode.

7. The method of claim 6, wherein, following the filling of the first electrode opening with the first electrode, the first electrode is formed by performing chemical mechanical polishing of a material used for the first electrode until the interlayer insulating film is exposed.

8. The method of claim 6, wherein following the filling of the second electrode opening with the second electrode, the second electrode is formed by performing chemical mechanical polishing of a material used for the second electrode until the interlayer insulating film and the first electrode are exposed.

9. The method of claim 8, wherein the dielectric layer on the first electrode and the interlayer insulating film is removed when performing chemical mechanical polishing to form the second electrode.

10. The method of claim 6, wherein the upper wiring is formed by forming an upper insulating film over the first electrode, the dielectric layer, the second electrode, and the interlayer insulating film, selectively etching the upper insulating film to form a wiring opening that exposes at least a portion of the second electrode, and filling the wiring opening with a metal material.

11. The method of claim 6, wherein the dielectric layer is formed by layering silicon oxide and silicon nitride.

12. The method of claim 6, wherein the first electrode and the second electrode are each formed to have a plurality of branches that extend from a base portion.